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June 8, 2000

By Facsimile (703) 308-7722

Examiner Michael Trinh/Art Unit 2822
 US Patent and Trademark Office

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Re: U.S. Patent Application Serial No. 09/059,644

Filed: April 13, 1998

**"Semiconductor Processing Methods of Forming a
 Conductive Gate and Line"**

Inventor: Pai-Hung Pan

Our File No.: MI22-898

Dear Examiner Trinh:

Thank you for your telephone call today regarding the missing Supplemental IDS, Form 1449 and accompanying art. As I reviewed our file, I discovered that there were two supplemental IDS filings, a first on April 18, 2000 and a second on May 9, 2000. To insure that I supply you with the correct papers, I am attaching both filings. As we discussed, you will find copies of the two Japanese patents that were included in the second IDS filing. All the art cited in the first filing and the balance of the art cited in the second filing are U.S. patents, of which you indicated that you will secure copies. For the record, I am also attaching copies of our postcards filed with each of the IDS filings. These postcards indicate the date each filing was received at the U.S. PTO.

Thank you for your help in this matter.

Best regards,



Bernard Berman

BB/cb

Enclosures: IDS w/PTO-1449; Supplemental IDS W/PTO-1449; Japanese patents (2);
 copies of two postcards

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